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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/749,792	12/28/2000	Zhong-Ning (George) Cai	2207/10615	6261

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EXAMINER	
CHEN, TSE W	
ART UNIT	**PAPER NUMBER**
2116	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Advisory Action After the Filing of an Appeal Brief	Application No. 09/749,792	Applicant(s) CAI, ZHONG-NING (GEORGE)	
	Examiner Tse Chen	Art Unit 2116	

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

The reply filed 03 April 2006 is acknowledged.

1. ☐ The reply filed on or after the date of filing of an appeal brief, but prior to a final decision by the Board of Patent Appeals and Interferences, will not be entered because:

   a. ☐ The amendment is not limited to canceling claims (where the cancellation does not affect the scope of any other pending claims) or rewriting dependent claims into independent form (no limitation of a dependent claim can be excluded in rewriting that claim). See 37 CFR 41.33(b) and (c).

   b. ☐ The affidavit or other evidence is not timely filed before the filing of an appeal brief. See 37 CFR 41.33(d)(2).

2. ☐ The reply is not entered because it was not filed within the two month time period set forth in 37 CFR 41.39(b), 41.50(a)(2), or 41.50(b) (whichever is appropriate). Extensions of time under 37 CFR 1.136(a) are not available.

   Note: This paragraph is for a reply filed in response to one of the following: (a) an examiner's answer that includes a new ground of rejection (37 CFR 41.39(a)(2)); (b) a supplemental examiner's answer written in response to a remand by the Board of Patent Appeals and Interferences for further consideration of rejection (37 CFR 41.50(a)(2)); or (c) a Board of Patent Appeals and Interferences decision that includes a new ground of rejection (37 CFR 41.50(b)).

3. ☒ The reply is entered. An explanation of the status of the claims after entry is below or attached.

4. ☒ Other: *Claims 1-20 remain rejected with supplemental Examiner's Answer provided.*

DETAILED ACTION

Responsive to the Reply Brief filed on April 3, 2006, a supplemental Examiner's Answer is set forth below.

Appellant alleges that McDermott "does not even remotely suggest an input that relates to a level of demand for performance in a processor" with the assertion that "a 'performance demanding level input' in a processor, by its terms, is an input that relates to a level of performance of the processor in accordance with demand". Examiner strongly disagrees and submits the following:

1. The original disclosure submitted on December 28, 2000 explicitly defines the performance demanding level signal (PDL) as "an input signal used by the frequency reduction circuit 305 to determine the level of sensitivity (or aggression) used for frequency reduction" [pg.7, ll.8-10]. Examiner submits that the signals LVL1 and LVL2 disclosed in McDermott for controlling the rate of frequency change [i.e., level of sensitivity in frequency reduction; col.4, l.66 – col.5, l.24; col.6, ll.51-64; col.8, l.45 – col.9, l.13] fits the explicit definition of the term as provided in the original disclosure.
2. The relation between PDL and "a level of performance of the processor in accordance with demand" is described in the disclosure [pg.7, l.16 – pg.8, l.2] as examples ["can be used" and "e.g."] with explicit declaration of the case by Appellant in the Remarks filed February 17, 2004 [pp.8-9]. As such, Examiner submits that the "narrower" example limitation of the PDL relating to "a level of performance of the processor in accordance with demand" in the disclosure cannot be read into the claims.

Accordingly, all subsequent arguments of the PDL "based on a demand for performance at a given level in a processor as called for in the claim on appeal" are deemed not persuasive.

Appellant alleges that "the sole purpose of McDermott's invention is to assure that the frequency of the system clock does not change". Examiner strongly disagrees and submits that McDermott's invention does support the generation of different frequencies [i.e., changing frequencies] [col.14, ll.16-25]. In essence, McDermott's invention provides the advantage of having a fast response time to input frequency changes ***as well as*** highly stable behavior that is most relevant to clock frequency reduction processes. The signals LVL1 and LVL2 disclosed in McDermott are used to stably control the advancing or retarding rate of change to the new desired frequency [col.14, l.67 – col.15, l.13; col.16, ll.24-46]. Such advantageous teaching does not advocate the prevention of clock frequency changes as the Appellant alleges [i.e., making stable frequency changes does not mean NO frequency changes].

Appellant questions the comments on pp.10, ll.9-12 of the previous Examiner's Answer concerning the "effective synchronization scheme". The comments were provided to link Appellant's concession that McDermott does teach the synchronization of a PLL to the advantage that such teachings of an "effective synchronization scheme" can be used in any systems involved in frequency reduction as in the case of primary reference Georgiou. An "effective synchronization scheme" is important in a system of frequency reduction because any changes in frequency ultimately requires synchronization in order to ensure the desired frequency and phase has been reached for the system to continue operation [i.e., changing frequencies haphazardly without synchronization would result in data mislatches and other processing errors].

Appellant asserts that "the PLL disclosed in the Appellant's application is distinct from the performance demanding level input is a clear indication that a PLL is not involved with and is irrelevant to the performance demanding level". Examiner submits that Appellant's assertion is consistent with Examiner's comment that "PLLs are commonly used in frequency controls such as throttling or frequency reduction, including Appellant's claimed apparatus that also employs a PLL... ***in the frequency control process***" [Examiner's Answer: pg.11, ll.15-18]. Examiner was providing support for the common inclusions of PLLs in ***frequency control processes*** and not the association of a performance demanding level input to a PLL [i.e., they are separate components that can be configured in a variety of ways in a ***frequency control process***].

Appellant may file another reply brief in compliance with 37 CFR 41.41 within two months of the date of mailing of this supplemental examiner's answer. Extensions of time under 37 CFR 1.136(a) are not applicable to this two month time period. See 37 CFR 41.43(b)-(c).

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

Tse Chen

LYNNE H. BROWNE
SUPERVISORY PATENT EXAMINER
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A Technology Center Director or designee has approved this supplemental examiner's answer by signing below:

Jack B. Harvey, Director
Technology Center 2100